

A MAGNETIC MEMORY DEVICE

Field of the Invention

5           The present invention relates to magnetic memory devices, and more specifically to methods of and structures for storing data in a magnetic memory device.

Background of the Invention

10           Non-volatile magnetic random access memory (MRAM) devices have the potential to replace volatile dynamic random access memory (DRAM) devices and static random access memory (SRAM) devices in some applications. The MRAM devices comprise arrays of cells operating on  
15   tunneling magneto-resistance (TMR), colossal magneto-resistance (CMR), and giant magneto-resistance (GMR) technology.

          MRAM cells are typically structured around "data" and "reference" layers. The data layer includes a writeable  
20   magnetic material, and the reference layer includes a fixed magnetic material. A dielectric layer in between the two has greater or lesser resistance to electrical current depending on whether the magnetic fields from the sandwiching layers are canceling or reinforcing one  
25   another.

          During a write operation, the magnetization of the data layer can be switched between two opposite states by applying an electro-magnetic field through a nearby wire loop. Thus binary information can be stored. The  
30   reference layer usually comprises a magnetic material in which the magnetization is pinned. A magnetic field applied to the data layer penetrates the reference layer

with insufficient strength to switch the magnetization in the reference layer.

For example, in a TMR cell, the data layer and the reference layer are separated by a thin dielectric layer so that a tunneling junction is formed. The probability that electrons will be able to tunnel through the dielectric layer depends on the direction of the magnetization in the data layer relative to the direction of the magnetization in the reference layer. Therefore, the structure is "magneto-resistant" and information can be stored and retrieved by reading the magnitude of tunneling currents thereafter able to pass through the memory cell.

In general, it is of advantage that the magnetic memory cells are as small as possible to increase memory density and reduce cost. However, as cells become smaller, thermal stability issues become more important. To ensure that stored information is not lost because of random switching induced by environmental influences, it is necessary that the data layers of small magnetic memory cells are such that the magnetic field strength that is required for switching the magnetization is higher than that for larger memory cells. Unfortunately the necessity to generate the larger fields strength makes switching of the memory cells during the write operation more difficult.

It is known that increasing the temperature of the magnetic memory cell lowers the magnetic field strength that is required for switching. Further, when an electrical current passes through the magnetic memory cell, heat is developed in the cell. However, the developed heat is easily conducted through the bit lines

away from the memory cell and therefore cannot be utilized to facilitate switching of the magnetic memory cell.

There is therefore a need for a magnetic memory device in which loss of heat from the magnetic memory cell  
5 is reduced and therefore the heat can be utilized to facilitate switching.

### Summary of the Invention

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Briefly, a magnetic random access memory (MRAM) embodiment of the present invention comprises a magnetic memory cell switchable between two states of differing electrical resistance of an interposing dielectric layer under the  
15 influence of a magnetic field. The MRAM also comprises a wire that is connected to the magnetic memory cell. The conductive line has a conductive connecting link and a conductive word or bit line which are electrically connected to each other. The connecting link is disposed  
20 between the word or bit line and the magnetic memory cell and has a thermal resistance that is larger than that of the word or bit line so as to provide a barrier for heat conduction from the magnetic memory cell to the word or bit line.

25 The invention will be more fully understood from the following description of embodiments of the invention. The description is provided with reference to the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a perspective diagram of a magnetic memory device according to an first embodiment of the present invention;

Fig. 2 is a perspective diagram of a magnetic memory device according to a second embodiment of the present invention; and

Fig. 3 is a perspective diagram of a magnetic memory device according to third embodiment of the present invention.

Detailed Description of Embodiments

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Fig. 1 represents a first magnetic random access memory (MRAM) embodiment of the present invention, and is referred to herein by the general reference numeral 100. The MRAM 100 comprises a number of individual magneto-resistance memory cells 102. In this case each memory cell 102 is a tunneling magneto resistance memory (TMR) cell. Each memory cell 102 comprises a magnetic reference layer 104, a dielectric layer 106 and a magnetic data layer 108. The device comprises electrically conductive word lines 110 and 112, respectively. These are typically metal, e.g., aluminum or copper. Both of which materials are good heat conductors.

The word lines 110 and 112 can heat sink memory cells 102 pretty effectively, and any localized heating could be carried away quickly. But if some of this local heating was allowed to pile at each active memory cell 102, the heat can be used to make switching the data layer 108 a

bit easier. And so in lies the present invention.  
Therefore a connecting link 114 has a narrowed neck that  
reduces the thermal path to the metal in word lines 110  
and 112. The connecting links 114 are formed as cones or  
5 pyramids.

The MRAM 100 comprises wires such as word lines 110  
and 112 having connecting links and word or bit lines,  
which in this example, are connecting links 114 and rails  
116 respectively. The connecting links have a thermal  
10 resistance that is larger than that of the word or bit  
lines so that a barrier for heat conduction is provided.  
In this example, the connecting links 114 are surrounded  
by a low thermal conductivity material, e.g.,  $\text{SiO}_2$ . A heat  
barrier is established because of the reduced cross-  
15 sectional area of the connecting links 114 through which  
heat can be conducted. Consequently more of the heat  
generated by the memory cell can be utilized to facilitate  
switching of the magnetic memory cell 114.

Each magnetic memory cell 102 is also connected to a  
20 bit line so that the magnetic memory cells are disposed  
between word lines 110 and 112 and bit lines 118. For  
clarity only one bit line 118 is shown.

The data layer 108 includes a magnetic material which  
is selected so that the direction of the magnetization is  
25 switchable as a function of an applied magnetic field. In  
general, MRAM 100 is such that the magnetization in the  
data layer 108 can have two opposing directions so that  
binary information can be stored as a function of the  
direction of the magnetic field generated by the current  
30 applied to bit line 118 and/or word line 104. When a  
current is applied along a bit line and/or a word line, a  
magnetic field will surround the bit line and/or word line

which can be utilized to switch the magnetization of the data layer 108.

Fig. 1 schematically indicates a circuit unit 120 that in use generates the write current through the bit line 118. The circuit may also generate a write current through the word lines 110 and 112. For clarity, electrical connections to the circuit unit 120 are not shown for word lines 110 and 112. Each magnetic memory cell may comprise a number of additional layers which are not shown for simplicity.

Dielectric layer 106 is thin enough so that, when a suitable electrical potential is applied between word line 110 or 112 and bit line 118, a tunneling current will flow through the dielectric layer 106. The tunneling probability and therefore the effective resistance of the memory cell depends on the direction of the magnetization in the data layer 108 relative to that of the reference layer 104. Therefore, it is possible to determine the orientation of the magnetization in the data layer from the tunneling current which is dependent on the resistance of the memory cell 102.

MRAM 100 further includes a read circuit for sensing the resistance of selected memory cells 102 during read operations. During read operations, a constant supply voltage or a ground potential is applied across the magnetic memory cells 102. The constant supply voltage may be provided by an external circuit. The read circuit is not shown in order to simplify the description.

MRAM 100 may comprise an array having any number of memory cells 102 arranged in any number of rows and columns. Further, MRAM 100 may comprise other magnetic memory cells such as colossal magneto resistance memory

cells (CMR) or giant magneto resistance memory (GMR) cells.

The connecting links 114 may include aluminum, tungsten, copper, amorphous carbon, doped amorphous or  
5 doped poly-crystalline silicon, or any conductive material. A possible material is an electrically conductive amorphous material, such as amorphous silicon or amorphous carbon, owing to the higher thermal resistivity of the amorphous state. Each connecting link  
10 114 has a reduced area top-surface that is, in this example, in contact with a reference layer of a respective magnetic memory cell. It will be appreciated that the connecting links 114 may not be in contact with the magnetic material of the magnetic memory cells 102. For  
15 example, layers of further material may be disposed between the connecting links 114 and the magnetic material of respective magnetic memory cells 102.

Alternatively the connecting links 114 need not be pyramidal shape, but may have any other suitable shape  
20 including conical or generally cylindrical shapes or shapes that approximate that of rectangular prisms which project from the rails such as 114 and 116. Word lines 110 and 112 may also operate as bit lines. Each magnetic memory cell may comprise a number of additional layers  
25 such as capping, AF and seed layers.

In a specific example of this embodiment, the connecting links 114 have a height of approximately 100nm and a base area of approximately 150 x 150nm. Each contact surface between the magnetic memory cells 302 and  
30 the connecting links 114 has an area of less than approximately 50 x 50, and possibly as small as 10 x 10nm. The word lines 110 and 112 may comprise copper and each word line 110 or 112 together with respective connecting

links 114 may be integrally formed. In this example, however, the connecting links 114 may comprise doped amorphous silicon.

Here, the data layer 108 includes nickel iron (NiFe),  
5 the reference layer 104 includes cobalt iron (CoFe) and the dielectric layer 106 includes  $\text{Al}_2\text{O}_3$ . These layers have the same planar area of approximately  $150\text{nm} \times 300\text{nm}$ , and the reference layer 104, the data layer 108 and the dielectric layer 106 have a thickness of approximately  
10  $3.5\text{nm}$ ,  $3\text{nm}$ , and  $1.2\text{nm}$  respectively.

The connecting links 114 may be fabricated by using conventional via processing techniques and adjusting the via etch parameters to selectively lateral etch the top of the via more than the base of the via. Initially copper  
15 lines 110 and 112 are fabricated using a copper damascene processes. A layer of conducting via material such as doped amorphous silicon and approximately  $100\text{nm}$  thick, is deposited over the patterned bit lines. A positive resist photolithography process is used to define the location  
20 and size of the pyramids. This is followed by an isotropic etch process that will result in a pyramidal structure. A thick layer of  $\text{SiO}_2$  is deposited and chemical-mechanically polished (CMP) to yield a flat surface with the tops of the pyramids exposed to make  
25 contact to the memory cells 102. The memory cell layers 104, 106, and 108 are deposited and the fabrication process is completed.

Fig. 2 shows a second embodiment of the MRAM device. Fig. 2 shows a of the device 200 comprising magnetic  
30 memory cells 202. Each magnetic memory cell comprises a reference layer 204, a dielectric layer 206 and a data layer 208. The structure and composition of the magnetic memory cells 202 is analogous to that of magnetic memory

cells 102 shown in Fig. 1 and discussed above. The device comprises wires such as word lines 210 and 212 having connecting links and word or bit lines, which in this example, are vias 214 and rails 216 respectively. The  
5 vias 214 are conductive and may comprise aluminum, tungsten, copper, amorphous carbon, doped amorphous or doped poly-crystalline silicon, etc. In this embodiment, each via 214 is positioned around a cylinder of insulating material. It will be appreciated that the vias 214 may  
10 not be in contact with the magnetic material of the magnetic memory cells 202. For example, layers of other material may be disposed between vias 214 and the magnetic material of respective magnetic memory cells 202.

It will also be appreciated that alternatively via  
15 214 may be of any other tubular shape including shapes that have a rectangular cross-sections. The word lines 210 and 212 may also operate as bit lines. Further, each magnetic memory cell may comprise a number of additional layers such as capping, AF and seed layers.

20 In an example of this embodiment, the vias 214 have a height of approximately 100nm and a diameter of less than approximately 150nm. Each contact surface between the magnetic memory cells 202 and the pyramids 214 has an area of less than approximately 50 x 50nm and possibly as  
25 small as 10 x 10nm. The word lines 210 and 212 may comprise copper and the vias 214 may comprise doped silicon and are centered around a core cylindrical core of SiO<sub>2</sub>.

The vias 214 may be fabricated using a combination of  
30 known semiconductor processing methods including spacer fabrication and chemical-mechanical polishing. For example, first a layer of electrically and thermally insulating material, such as SiO<sub>2</sub>, is deposited to a

thickness at least as great as the final desired thickness of the via 214. This layer is then patterned into cylindrical regions on top of word lines 210 and 212 using standard photolithographic and etching processes. A  
5 conductive spacer is then formed around the perimeter of the cylindrical region by first depositing a conformal layer of conductive material. Then using an anisotropic etch to remove the conductive material everywhere except from the vertical side walls of the cylindrical regions.  
10 A thick layer of  $\text{SiO}_2$  is deposited and chemical-mechanically polished (CMP) to yield a flat surface with the tops of the vias exposed to make contact to the memory cells 202. The memory cell layers 204, 206, and 208 are deposited and the fabrication process is completed. In  
15 this manner memory cells 202 are electrically connected to word lines 210 and 212 through vias 214.

The device 200 comprises an array of the magnetic memory cells and a plurality of electrically bit lines and word lines each connected to a plurality of magnetic  
20 memory cells. The device 200 also comprises bit lines and circuitry such as 110 which is for clarity not illustrated in Fig. 2.

Referring now to Fig. 3, a MRAM embodiment of the present invention is referred to herein by the general  
25 reference numeral 300. MRAM 300 includes an array of magnetic memory cells 302. Each magnetic memory cell 302 comprises a magnetic reference layer 304, a tunneling dielectric layer 306 and a magnetic data layer 308. Each word line has two parts, a high conductivity backing rail  
30 310 and 312, and a lower conductivity cell contacting rail 311 and 313. These are disposed within electrically and thermally insulating substrates 314 and 316.

Although connecting links 311, 313 and word or bit lines 310, 312 are shown having equal widths in Fig. 3, the two can have different cross sectional geometries and materials.

5           To simultaneously minimize thermal conduction from the memory cell and maintain high electrical conductivity along the word lines, the width of the connecting links may be substantially smaller than the widths of the word or bit lines. For example, the connecting rail facings  
10   311 and 313 can have a height and width of approximately 100nm and 10nm respectively, and the word or bit lines 310 and 312 have a height and width of approximately 200nm and 200nm respectively. The tops of the connecting rail facings 311 and 313 are in contact with respective  
15   reference 304 layer of respective magnetic memory cells 302. As the connecting rail facings 311 and 313 have only a relatively small cross-sectional area through which heat can be conducted to the word or bit lines 310 and 312, heatsinking from the magnetic memory cells 302 can be  
20   reduced. Consequently, more of the heat generated by the memory cell will linger to facilitate data switching.

          The connecting links may comprise doped amorphous silicon which has a higher thermal resistance than copper, and further reduces the loss of heat. The word or bit  
25   lines 310 and 312 may comprise copper which has a relatively low electrical resistance and the word or bit lines carry a larger current than the connecting rail facings 311 and 313.

          It will be appreciated that alternatively the  
30   connecting rail facings 311 and 313 may not be in contact with the magnetic material of the magnetic memory cells 302. For example, layers of further material may be disposed between the magnetic material of the magnetic

memory cells 302 and the connecting rail facings 311 and 313. In addition, it will be appreciated that alternatively the word lines may also operate as bit lines.

5           Here, the data layer 308 includes nickel iron (NiFe), the reference layer 304 includes cobalt iron (CoFe) and the dielectric layers 306 may comprise  $\text{Al}_2\text{O}_3$ . These layers have the same planar area of approximately  $150\text{nm} \times 300\text{nm}$ , and the reference layer 304, the data layer 308 and the  
10       dielectric layer 306 have a thickness of approximately  $3.5\text{nm}$ ,  $3.0\text{nm}$ , and  $1.2\text{nm}$  respectively.

          One method of manufacturing a bit line such as 310 and 312 includes the following steps. Initially a channel is etched into a dielectric substrate. Then the  
15       dielectric substrate and the interior of the channel are coated with a metallic material such as copper so as to fill the channel. A thin diffusion barrier or adhesion layer of a material such as Ta or TaN may precede the copper deposition. A chemical-mechanical polishing  
20       process is then used to planarized the copper line and the surrounding dielectric. A second dielectric material is then deposited over the planarized surface and etched into a channel such that one edge of the channel is positioned on top of, and parallel to, an underlying copper line.  
25       The second edge of the channel may be positioned on top of an adjacent copper line. Then the top surface of the second dielectric, the interior of the channel and the exposed Copper surface are coated with an electrical conductor that is a poor thermal conductor, such as doped  
30       amorphous silicon. In an anisotropic etch process, silicon is etched away from all areas except the channel walls so that silicon strips are formed. The channel is then filled with a third dielectric material and a

chemical-mechanical polishing process is again used to planarize the silicon strips and surrounding dielectrics. On the planar structure magnetic memory cells are formed so that the memory cells are connected to edges the  
5 silicon strip.

Each magnetic memory cell 302 may comprise a number of additional layers such as capping, AF and seed layers. The MRAM 300 comprises an array of the magnetic memory cells and a plurality of bit lines and word lines, each  
10 connected to a plurality of magnetic memory cells. Further, the MRAM 300 also comprises bit lines and circuitry which is for clarity not illustrated in Fig. 3.

In general, the word or bit line may have a relatively low electrical resistance and may be suitable  
15 to carry a relatively large current. The connecting link may be shaped so as to cause the thermal resistance of the connecting link to be greater than that of the word or bit line and the thermal barrier may be established by reducing the cross-sectional area of the connecting link  
20 though which heat can be conducted from the magnetic memory cell to the second. Areas adjacent the connecting link may comprise a thermally and electrically insulating material. Alternatively or additionally the connecting link may comprise a material that is of a thermal  
25 resistivity higher than that of the word or bit line. For example, the connecting link may comprise amorphous silicon.

The resistance of the connecting link is preferably less than 10% of that of the magnetic memory cell itself.  
30 The connecting link is of a relatively low electrical resistance, which has electrical advantages, while providing a barrier for heat. The connecting links and

word or bit lines may be connected to each other or may be integrally formed.

The wire may be a bit line. The wire may be a word line. The wire may also be one of two or more lines, for  
5 example, a bit line and a word line may be connected to the magnetic memory cell. The magnetic memory cell may has opposite faces and the conductive lines are connected to the opposite faces.

The connecting link may be in electrical contact with  
10 the magnetic memory cell. Alternatively, at least one layer may be disposed between the connecting link and the magnetic memory cell.

For example, the word or bit line may have a peripheral surface and the connecting link may be a link  
15 that projects towards the magnetic memory cell. In this case heatsinking can be reduced by reducing the cross-sectional area of the link through which the heat can be conducted and may be further reduced if the link comprises a material that has a thermal resistivity higher than that  
20 of the word or bit line. The magnetic memory cell has a face to which the wire is connected and the link has a zone in which the cross-sectional area through which heat can be conducted is smaller than approximately 20% of the area of the face of the magnetic memory cell. The link  
25 may have a base surface that is connected to the word or bit line.

The connecting link and the word or bit line may be integrally formed. The link may be of a generally cone-like or pyramidal form. The link may be of a tubular  
30 shape. In this case, the link also comprises a cylindrical core comprising an insulating material around which the tubular link is positioned.

The wire may have a generally uniform cross-sectional shape along its length. The first and word or bit line may be parallel. The magnetic memory cell may have a base surface and the area within which the connecting link is  
5 connected to the magnetic memory cell may be smaller than the base surface. In this case heatsinking is reduced as the cross-sectional area of the connecting link through which the heat can be conducted is reduced. The magnetic memory cell has a face to which the wire is connected and  
10 the connecting link has a zone in which the cross-sectional area through which heat can be conducted is smaller than approximately 20% of the area of the face of the magnetic memory cell. Heatsinking may be further reduced if the connecting link comprises a material that  
15 has a thermal resistivity higher than that of the word or bit line.

The magnetic memory device typically is one of an array of the magnetic memory devices. The device comprises a plurality of wires each connected to a  
20 plurality of magnetic memory cells.

The magnetic memory device a magnetic random access memory (MRAM) device. The MRAM device may be any type of MRAM device such as a colossal magneto resistance (CMR) memory device or a giant magnetoresistance (GMR) memory  
25 device but is a tunneling magneto resistance (TMR) memory device. The magnetic memory cell comprises a magnetic data layer a magnetic reference layer and a dielectric layer sandwiched between the data layer with the layers being such that a tunneling junction is formed at the  
30 dielectric layer.

The present invention provides in another embodiment a magnetic memory device comprising a magnetic memory cell including a magnetic material switchable between two

states on the application of a magnetic field, a wire connected to the magnetic memory cell and disposed with an orientation that is chosen to reduce the conduction of heat from the magnetic memory cell into the wire.

5           The present invention provides in a further embodiment a magnetic memory device comprising an array of magnetic memory cells, each magnetic memory cell being switchable between two states of differing electrical resistance of an interposing dielectric layer under the  
10 influence of a magnetic field; and a plurality of wires; each conductive line connected to a plurality of magnetic memory cells and at least some of the wires having a conductive connecting link and a conductive word or bit  
15 connecting link being disposed between a respective word or bit line and at least some of the magnetic memory cells and having a thermal resistance that is larger than that of the word or bit line so as to provide a barrier for heat conduction from the magnetic memory cell to the word  
20 or bit line.

A plurality of links may project towards respective magnetic memory cells from each word or bit line. Alternatively, at least some of the wires which comprise the connecting links and word or bit lines may have a  
25 generally uniform cross-sectional shape along their length.

The present invention also provides in an embodiment a magnetic memory device comprising a magnetic memory cell including a magnetic material switchable between two  
30 states on the application of a magnetic field. A wire is connected to the magnetic memory cell, the wire being a strip that has an edge and a major surface, the edge connected to the magnetic memory cell.

Although the invention has been described with reference to particular examples, it will be appreciated by those skilled in the art that the invention may be embodied in many other forms. For example, the magnetic  
5 memory cells may be colossal magneto resistance memory cells (CMR) or giant magneto resistance memory (GMR) cells. Further, it will be appreciated that the respective low thermal conductivity connecting links may contact the magnetic memory cells not only from below as  
10 shown in the Figs., but alternatively or additionally from above. In addition, the low thermal conductivity connecting links may not contact the magnetic memory at the center of their bottom or top face, but alternatively contact may be established closer to an edge of a magnetic  
15 memory cell.

What is claimed is: